CLAIMS

1. A comparator offset calibration method for A/D converters, **characterized by**

providing, for each comparator in a comparator array, a common reference signal to both comparator input terminals;

forcing each comparator in said array into the same predetermined logical output state; and

adjusting, for each comparator in said array, the comparator trip-point until the logical output state is inverted.

2. The method of claim 1, **characterized by** adjusting each comparator trip-point by a monotonically varying signal.

3. The method of claim 1 or 2, **characterized by** simultaneously adjusting all comparators in said array by a common ramp signal.

4. The method of claim 1, 2 or 3, **characterized by** D/A converting, for each comparator in said array, a digital ramp signal into an analog trip-point adjustment signal.

5. The method of claim 4, **characterized by** storing, for each comparator in said array, an offset calibration coefficient representing the digital ramp signal value that inverts its logical output state.

6. The method of claim 4, **characterized by** storing, for each comparator in said array, an offset calibration coefficient representing the average of an increasing digital ramp signal value that inverts its logical output state and a decreasing digital ramp signal value that inverts its logical output state.

7. The method of claim 4, **characterized by**

repeating, for each comparator in said array, said adjustment step; and

storing, for each comparator in said array, an offset calibration coefficient representing the average of several digital ramp signal values that invert its logical output state.

8. The method of any of the preceding claims 5-7, **characterized by** storing, for each comparator in said array, said offset calibration value externally at A/D converter power-down for later retrieval at A/D converter startup.

9. A comparator offset calibration system for A/D converters, **characterized by**

means (CCU, SW1-SW7) providing, for each comparator in a comparator array, a common reference signal to both comparator input terminals;

means (CCU, DAC1-DAC7) for forcing each comparator in said array into the same predetermined logical output state; and

means (CCU, DAC1-DAC7) for adjusting, for each comparator in said array, the comparator trip-point until the logical output state is inverted.

10. The system of claim 9, **characterized by** means (CCU, DAC1-DAC7) for adjusting each comparator trip-point by a monotonically varying signal.

11. The system of claim 9 or 10, **characterized by** means (CCU, DAC1-DAC7) for simultaneously adjusting all comparators in said array by a common ramp signal.

12. The system of claim 9, 10 or 11, **characterized by** calibrating D/A converters (DAC1-DAC7) for D/A converting, for each comparator in said array, a digital ramp signal into an analog trip-point adjustment signal.

13. The system of claim 12, **characterized by** registers (REG1-REG7) for storing, for each comparator in said array, an offset calibration coefficient (CAL1-CAL7) representing the digital ramp signal value that inverts its logical output state.

14. The system of claim 12, **characterized by** registers (REG1-REG7) for storing, for each comparator in said array, an offset calibration coefficient representing the average of an increasing digital ramp signal value that inverts its logical output state and a decreasing digital ramp signal value that inverts its logical output state.

15. The system of claim 12, **characterized by**

means (CCU) for repeating, for each comparator in said array, said adjustment step; and

registers (REG1-REG7) for storing, for each comparator in said array, an offset calibration coefficient representing the average of several digital ramp signal values that invert its logical output state.

16. The system of any of the preceding claims 13-15, **characterized by** means for storing, for each comparator in said array, said offset calibration value externally at A/D converter power-down for later retrieval at A/D converter startup.

17. An A/D converter including at least one comparator array for flash A/D conversion of an analog signal, **characterized by**

means (CCU, SW1-SW7) providing, for each comparator in said array, a common reference signal to both comparator input terminals;

means (CCU, DAC1-DAC7) for forcing each comparator in said array into the same predetermined logical output state; and

means (CCU, DAC1-DAC7) for adjusting, for each comparator in said array, the comparator trip-point until the logical output state is inverted.

18. The converter of claim 17, **characterized by** means (CCU, DAC1-DAC7) for adjusting each comparator trip-point by a monotonically varying signal.

19. The converter of claim 17 or 18, **characterized by** means (CCU, DAC1-DAC7) for simultaneously adjusting all comparators in said array by a common ramp signal.

20. The converter of claim 17, 18 or 19, **characterized by** calibrating D/A converters (DAC1-DAC7) for D/A converting, for each comparator in said array, a digital ramp signal into an analog trip-point adjustment signal.

21. The converter of claim 20, **characterized by** registers (REG1-REG7) for storing, for each comparator in said array, an offset calibration coefficient (CAL1-CAL7) representing the digital ramp signal value that inverts its logical output state.

22. The converter of claim 20, **characterized by** registers (REG1-REG7) for storing, for each comparator in said array, an offset calibration coefficient representing the average of an increasing digital ramp signal value that inverts its logical output state and a decreasing digital ramp signal value that inverts its logical output state.

23. The converter of claim 20, **characterized by**

means (CCU) for repeating, for each comparator in said array, said adjustment step; and

registers (REG1-REG7) for storing, for each comparator in said array, an offset calibration coefficient representing the average of several digital ramp signal values that invert its logical output state.

24. The converter of any of the preceding claims 21-23, **characterized by** means for storing, for each comparator in said array, said offset calibration value externally at A/D converter power-down for later retrieval at A/D converter startup.

25. The converter of any of the preceding claims 15-21, **characterized in** that the comparators in said array comprise regenerative latches.